IN THE SPECIFICATION

Replace page 5, line 27 through page 6, line 16 with the following:

The detected voltage is supplied to a comparator CMP and is compared with an output level instruction signal Vramp supplied from a baseband circuit or a control circuit such as a microprocessor. A voltage or current according to the input potential difference is supplied to a bias generating circuit BIAS where a gate bias voltage for the power amplification transistor TR3 is generated, thereby controlling the output level. In FIG. 7, C1 denotes a ~~capacitative~~ capacitive element for blocking a direct current component of the input high frequency signal Pin, and MN4 indicates an impedance matching circuit for performing matching so that an impedance at an output terminal becomes 50Ω. The power amplification transistor TR3 may be provided, not necessarily in one stage, in a plurality of stages.

Replace page 9, lines 16 through page 10, line 4 with the following:

In a high frequency power amplification electric part as a component of a wireless communication system which detects an output level necessary for feedback control of output power by a current detecting method, a ~~capacitative~~ capacitive element is interposed between the drain terminal of a power amplification transistor in the final stage and a proper node such as the gate terminal of a transistor constructing a current mirror circuit in a circuit for detecting an output level, and a change in the output power accompanying load fluctuation is transmitted to the inner node of the output level detecting circuit via the ~~capacitative~~ capacitive element and is reflected in a detection current of the output level detecting circuit.

Replace page 10, lines 16-25 with the following:

The ~~capacitative~~ capacitive element for reflecting a change in the output power into the detection current of the

output level detecting circuit has, preferably, a capacitance value of 1 pF or larger. When the capacitance value is too small, fluctuation in the output power accompanying load fluctuation cannot be sufficiently transmitted to a feedback control system, so that the fluctuation in the output power cannot be suppressed to a desired level or less.

Replace page 10, line 26 through page 11, line 12 with the following:

On the other hand, when the capacitance value is too large, it is not preferable for the following reason. Change in the output power is further added to a relatively small change in an output level detected from an input signal when the output power level is low. The feedback control system excessively reacts with the fluctuation in the output power. In addition, it becomes difficult to reduce the size of a semiconductor chip and a module. A proper maximum value of the ~~capacitative~~ capacitive element for transmitting change in the output power is, although it depends on the constant of a device of the circuit and the like, about 2 to 4 pF.

Replace page 13, line 11 through page 14, line 4 with the following:

FIG. 1 schematically shows a transmission circuit examined by the inventor herein and the others. Shown in FIG. 1 are: an antenna ANT for transmission/reception; an output power amplifier PA for amplifying an input high frequency signal Pin and driving the antenna ANT, constructed by three amplification stages which are cascaded; a transistor TR3 for power amplification serving as the final amplification stage; an inductance element L1 connected between a power source voltage terminal Vdd1 and the drain terminal of the transistor TR3 for power amplification; an impedance matching circuit MN4; a ~~capacitative~~ capacitive element CDC4 for blocking a direct current component; a low pass filter LPF for blocking harmonics components of a transmission signal, a transmission/reception change-over switch SW; and a branching filter DIS for branching a reception signal into a GSM signal of 900 MHz or the like and a DCS signal of 1800 MHz or the like.

Replace page 19, line 1-18 with the following:

In FIG. 3, CDC1, CDC2, and CDC3 denote ~~capacitative~~ capacitive elements for blocking a direct current component, and MN1 to MN4 indicate impedance matching circuits constructed by capacitors CP1 to CP6 and transmission lines TL1 to TL7. The size (gate width) of the transistor TR4 for output detection is set to a fraction of tens of the size of the transistor TR3 for power amplification and it is designed so that the current of the transistor TR3 becomes few tens mA when the drain current Idd of the transistor TR3 for power amplification is a few A (Ampere). The size ratio between the transistors TR5 and TR6 for a current mirror is almost 1:1. With the configuration, the current flowing in the output level detection circuit ODT is set to a value much smaller than the drain current Idd of the transistor TR3 for power amplification.

Replace page 26, line 17 through page 27, line 3 with the following:

In the case of forming the capacitor C3 of which capacitance value is 1 pF or the like by using the dielectric layer of which dielectric constant Er = 8.854×10^{-12} F/m (specific inductive capacity S = 9) on the module substrate, if the thickness (distance between electrodes) t of the dielectric layer is 50 μm, the occupation area S is 6.4 mm^2 from C= Er·S/t. The length of one side in the case of the capacity of a rectangular shape is about 0.8 mm. Therefore, a ~~capacitative~~ capacitive element of such a size can be sufficiently formed on the module substrate. Thus, the whole module can be constructed more compactly than the case of using a discrete part as the capacitor C3.

Replace page 34, lines 7-22 with the following:

Electrodes on the top face of the semiconductor chips IC1, IC2, and IC3 and the predetermined conductive layer 12 are electrically connected to each other via bonding wires 31. On the surface of the first dielectric layer 11, the conductive pattern 12a constructing microstrip lines MS7, MS8,

and the like are formed and a plurality of discrete parts 32 such as the ~~capacitative~~ capacitive elements CDC1 to CDC4 and CP1 to CP6 and resistive elements R1 and R4 for constructing the power amplification circuit, the output level detecting circuit, and the like are mounted. Among the elements, the ~~capacitative~~ capacitive elements can be formed in the board by using the conductive layers on the surfaces and back faces of the dielectric layers 11 without using discrete parts.